

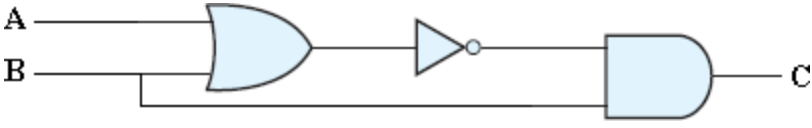
DEPARTMENT OF BIOMEDICAL ENGINEERING

QUESTION BANK

SUBJECT CODE/NAME : EC 8392/ DIGITAL ELECTRONICS

YEAR / SEMESTER : II / IV

UNIT I DIGITAL FUNDAMENTALS			
Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization and Quine-McCluskey method of minimization.			
PART A			
Q. No	Questions	BT Level	Domain
1.	Express the function $Y = A + \overline{BC}$ in canonical POS.	BTL 1	Remembering
2.	Convert the given decimal numbers to their binary equivalent 108.364, 268.025.	BTL 3	Applying
3.	Why totem pole outputs cannot be connected together?	BTL 2	Understanding
4.	Convert $(115)_{10}$ and $(235)_{10}$ into hexadecimal numbers.	BTL 1	Remembering
5.	Define 'Minterm' and 'Maxterm'.	BTL 4	Analyzing
6.	Draw an active high tri-state Gate & write its truth table.	BTL 2	Understanding
7.	Show how to connect NAND gates to get an AND gate and OR gate?	BTL 1	Remembering
8.	State Distributive law and Duality principle.	BTL 3	Applying
9.	What is meant by Prime Implicant and Essential prime implicants?	BTL 2	Understanding
10.	Find the minimized Boolean expression of this function $F=XY+X(Y+Z) +Y(Y+Z)$.	BTL 1	Remembering
11.	Find the canonical POS form of $Y= A+B'C$	BTL 1	Remembering

12.	Implement $Y = \sum(1,4,5,6,7)$ in SOP form using AOI logic.	BTL 6	Creating
13.	Determine the Boolean expression for the output of the system shown in figure. 	BTL 5	Evaluating
14.	Simplify: $\overline{ABC} + \overline{\overline{ABC}}$ using Boolean theorems.	BTL 4	Analyzing
PART – B			
1.	(i) Find the Minimized logic function using K-Maps and Realize using NAND and NOR gate. $F(A, B, C, D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$. (8)	BTL 1	Remembering
	(ii) Show that if all the gate in a two-level OR-AND gate network are replaced by NOR gate, the output function does not change. (5)	BTL 2	Understanding
2.	(i) Illustrate the MSOP representation for $F(A,B,C,D,E) = m(1,4,6,10,20,22,24,26) + d(0,11,16,27)$ using K-map method. Draw the circuit of the minimal expression using only NAND gates. (7)	BTL 2 BTL 1	Understanding Remembering
	(ii) Write about Excess 3 and Gray Code with an example. (6)		
3.	(i) Develop the given function $Y(M, N, O, P, Q) = \sum m(0,2,4,6,9,13,21,23,25,29,31)$. Draw the K-map and Implement the simplified expression using basic gates. (8)	BTL 4	Analyzing
	(ii) Implement $F = A'B'D' + B'C' + E'$ using NAND gates. (5)		
4.	Evaluate the following Boolean expression using Boolean Algebra and draw the logic diagram.	BTL 5	Evaluating
	(i) $T(X, Y, Z) = (X + Y)(\overline{X(Y + Z)}) + XY + XZ$. (5)		
	(ii) $\overline{XYZ} + \overline{XYZ} + XY$ (4)		
	(iii) $\overline{XYZ} + \overline{XZ} + \overline{YZ}$ (4)		
5.	(i) Why does a good logic designer minimize the use of NOT gates? (3)	BTL 2 BTL 4	Understanding Analyzing
	(ii) Find a MinSOP and MinPOS for the following function $F = \overline{bcd} + bcd + a\overline{cd} + \overline{abc} + \overline{abcd}$. (10)		

6.	(i) Using K-map method, Simplify the following Boolean function $=\sum m(0,2,3,6,7) + d(8,10,11,15)$ and obtain (a) minimal SOP (6) (b) minimal POS expression & realize using only NAND and NOR gates. (7)	BTL 2	Understanding
7.	(i) Draw the multilevel two input NAND circuit for the following expression: $F = (\overline{AB} + \overline{CD})E + BC(A + B)$ (3) (ii) How would you express the Boolean function using K-map and draw the logic diagram $F(w,x,y,z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$. (10)	BTL 4 BTL 1	Analyzing Remembering
8.	(i) Simplify the following function using K – map, $F=ABCD+AB'C'D'+AB'C+AB$ & realize the SOP using only NAND gates and POS using only NOR gates. (8) (ii) Simplify the logic circuit shown in figure (5)	BTL 4	Analyzing
9.	Explain the minimization of the given Boolean function using Quine-Mc-Cluskey method $F = \sum m(0,1,2,5,7,8,9,10,13,15)$.Realize the simplified function using logic gates. (13)	BTL 1	Remembering
10.	(i) Explain the implement of the following function using NAND and inverter gates $F=AB+A'B'+B'C$. (5) (ii) Using K-map method, simplify the given Boolean function and obtain minimum POS expression. $X = \prod m(1,3,5,7,9) + \prod d(8,11,15)$. (8)	BTL 1	Remembering
11.	(i) Given $Y(A,B,C,D) = \prod M(0,1,3,5,6,7,10,14,15)$, Draw the K-Map and Obtain the simplified expression. Design the minimum expression using basic gates. (8) (ii) Construct the expression $Y(A, B, C) = \prod M(0,2,4,5,6)$ using Only NOR-NOR logic. (5)	BTL 6	Creating

12.	What are the advantages of using tabulation method? Develop the following Function using Tabulation method $F = \sum(1,2,3,7,8,9,10,11,14,15)$ and implement using only NAND (13)	BTL 3	Applying
13.	i. Convert $(725.25)_8$ to its decimal, binary and Hexadecimal equivalent. (6) ii. Find 1's and 2's Complement of 8 digit binary numbers 10101101 (7)	BTL 2	Understanding
14.	(i) Implement $Y = (A + C)(\overline{A + D})(\overline{A + B + C})$ (5) (ii) Solve by perfect induction (8) (a) $A + AB = A$ (b) $A(A+B) = A$ (c) $A + A'B = A + B$ and (d) $A(A'+B) = AB$	BTL 3	Applying
PART C			
1.	Design the given function using Prime implicant method and Verify your result using K map $F = \sum m(0,1,2,4,5,6,8,9,12,13,14)$ (15)	BTL 6	Creating
2.	A staircase light is controlled by two switches , one is at the top of the stairs and the other is at the bottom of the stairs : i. Make a truth table for this system. (3) ii. Write the logic function in SOP form. (3) iii. Realize the circuit using AOI logic. (4) Realise the circuit using minimum number of NAND and NOR gates. (5)	BTL 5	Evaluating
3.	Implement the following function using Quine McCluskey method $F = \sum m(0,1,2,8,9,15,17,21,24,25,27,31) + d(3,4,11)$ (15)	BTL 6	Creating
4.	Develop the simplified Boolean expression for $f(A,B,C,D,E) = \sum(0,5,6,8,9,10,11,16,20,24,25,26,27,29,31)$ (15)	BTL 5	Evaluating

UNIT II COMBINATIONAL CIRCUIT DESIGN

Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Multiplexer, Demultiplexer, Magnitude Comparator, Decoder, Encoder, Priority Encoder.

PART A

Q.No	Questions	BT Level	Domain
1.	Define Half adder and Full adder circuit.	BTL 1	Remembering
2.	Construct 4-bit parallel adder/subtractor using Full adders and EXOR gates.	BTL 6	Creating
3.	Relate carry generate, carry propagate, sum and carry-out of a carry look ahead adder.	BTL2	Understanding
4.	Write about the design procedure for combinational circuits.	BTL 1	Remembering
5.	Identify the basic principle used in order to check or generate the proper parity bit in a given code word.	BTL 3	Applying
6.	Distinguish between demultiplexer and decoder	BTL 4	Analyzing
7.	Convert a two-to-four line decoder with enable input to 1:4 demultiplexer.	BTL2	Understanding
8.	Write about the design procedure for combinational circuits.	BTL 1	Remembering
9.	Sketch the logic diagram and truth table for Full adder circuit.	BTL 3	Applying
10.	Compare the function of decoder and encoder.	BTL 2	Understanding
11.	Evaluate the logic circuit of a 2 bit comparator.	BTL 5	Evaluating
12.	Design the logic circuit of Half subtractor using truth table.	BTL 6	Creating
13.	State the function of select inputs of a MUX.	BTL 1	Remembering
14.	Develop the following function using suitable multiplexer $F = \sum m(0,2,5,7)$.	BTL 4	Analyzing
15.	How would you design the logic diagram of a 2 bit multiplier?	BTL 1	Remembering
16.	Draw the logic diagram of a serial adder.	BTL3	Applying
17.	Explain a 3 bit even parity generator.	BTL5	Evaluating
18.	Describe code converter? List their types.	BTL 2	Understanding
19.	Examine a single bit magnitude comparator to compare two words A and B.	BTL 4	Analyzing
20.	Convert gray code 101011 into its binary equivalent.	BTL 2	Understanding

PART – B

1.	(i) How will you design a full adder using two half adders and an OR gate. (5) (ii) Analyze the principle and design of Parallel multiplier with diagrams (8)	BTL 4	Analyzing
2.	(i) Design a 4-bit decimal adder using 4-bit binary adders. (7) (ii) Simplify the function using multiplexer $F = \sum (0,1,3,4,8,9,15)$. (6)	BTL 6 BTL 4	Creating Analyzing
3.	(i) Construct full subtractor using Demultiplexer. (6) (ii) Write short note on BCD adder. (7)	BTL 3 BTL 1	Applying Remembering
4.	(i) Analyze the design of 8 x 1 multiplexer using only 2 x 1 multiplexer. (6) (ii) Formulate the following Boolean function using 4 x 1 multiplexers. $F(A, B, C, D) = \sum (1,2,3,6,7,8,11,12,14)$. (7)	BTL 4 BTL 6	Analyzing Creating

5.	(i) Draw the logic diagram of a 2-bit by 2-bit binary multiplier and explain its operation. (6) (ii) Realize $F(w, x, y, z) = \Sigma (1,4,6,7,8,9,10,11,15)$ using 8 to 1 Multiplexer. (7)	BTL 3 BTL 2	Applying Understanding
6.	(i) Realize a circuit to carryout both addition and subtraction. (7) (ii) Deduce the design of a 1:8 demultiplexer circuit. (6)	BTL 2	Understanding
7.	How would you design (i) Full adder using demultiplexer. (7) (ii) Serial binary adder. (6)	BTL 1 BTL 4	Remembering Analyzing
8.	Illustrate BCD to excess 3 code converter using minimum number of NAND gates. (13)	BTL 2	Understanding
9.	(i) Explain the working and draw the logic diagram of Binary to Octal decoder. (6) (ii) How would you design BCD to Gray code converter. Use don't care. (7)	BTL 1	Remembering
10.	(i) Demonstrate 4-bit magnitude comparator with three outputs: $A > B$, $A = B$ and $A < B$. (7) (ii) Build a 4-bit Priority Encoder circuit using gates. (6)	BTL 2 BTL 3	Understanding Applying
11.	(i) Give a combinational circuit that converts 4 bit Gray Code to a 4 bit binary number. Implement the circuit. (8) (ii) Develop a Full adder using decoder. (5)	BTL 1 BTL 3	Remembering Applying
12.	(i) How would you design a 3:8 decoder using basic gates? (7) (ii) How would you design a binary to gray code convertor? (6)	BTL 1 BTL 4	Remembering Analyzing
13.	(ii) Describe the design of Binary Multiplier using Shift Add method. (6) (ii) Show the design of excess 3 to BCD code converter using minimum number of NAND gates (7)	BTL 1	Remembering
14.	(i) Estimate the logic diagram of BCD-Decimal decoder and explain its operations. (7) (ii) Interpret the design of a BCD to seven segment decoder with neat diagrams. (6)	BTL 5	Evaluating
PART C			
1.	With necessary diagrams, explain in detail about the working of a 4-bit look ahead carry adder. Also mention its advantages over conventional adder. (15)	BTL 5	Evaluating
2.	Implement the following Boolean function using an 8:1 multiplexer considering D as the input and A,B,C as selection lines : $F(A, B, C, D) = AB' + BD + B'CD'$ (15)	BTL 5	Evaluating

3.	Construct 4-bit binary multiplier and divider and explain its operation with suitable example. (15)	BTL 6	Creating
4.	(i). Design an even parity generator that generates an even parity bit for every input string of 3 bits. (10) (ii). Explain the need of Parity Checker circuit with necessary diagrams. (5)	BTL 6	Creating

UNIT III SEQUENTIAL CIRCUITS

Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, state minimization, state assignment, circuit implementation – Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register. .

PART A

Q. No	Questions	BT Level	Domain
1.	Bring out the difference between synchronous sequential circuits and asynchronous sequential circuits.	BTL 3	Applying
2.	Define the terms: state table and state assignment.	BTL 1	Remembering
3.	Construct the state diagram of Mod-10 ring counter and find the number of Flip Flops required.	BTL 5	Evaluating
4.	State the classification of Sequential circuits.	BTL 1	Remembering
5.	Realize JK Flip Flops.	BTL 5	Evaluating
6.	Analyze the differences between Latch and Flipflop.	BTL 4	Analyzing
7.	Build a T Flip-flop from a D Flip-flop.	BTL 3	Applying
8.	Illustrate the logic diagram of a clocked SR Flipflop.	BTL 3	Applying
9.	State the difference between Mealy and Moore state machines.	BTL 1	Remembering
10.	How does ripple counter differ from synchronous counter?	BTL 2	Understanding
11.	Point out the condition on JK FF to work as D FF.	BTL 4	Analyzing
12.	Model a NAND based logic diagram of Master Slave JK FF.	BTL 2	Understanding
13.	Build the state diagram and characteristics equation of a D FF.	BTL 6	Creating
14.	Find minimum number of flip-flops needed to design a counter of Modulus 60.	BTL 1	Remembering
15.	A binary ripple counter is required to count upto $16,383_{10}$. How many Flip Flops are required ? If the clock frequency is 8.192 MHz, What is the frequency at the output of MSB?	BTL 6	Creating
16.	What is the primary disadvantage of asynchronous counter?	BTL 1	Remembering

17.	Point out two differences between edge triggering and level triggering in sequential circuits.	BTL 4	Analyzing																																															
18.	Explain about D-Latch with truth table.	BTL 2	Understanding																																															
19.	How many flip-flops are required to build a binary counter that counts from 0 to 1023?	BTL 2	Understanding																																															
20.	Draw the state diagram for removing lockout in Counters.	BTL 1	Remembering																																															
PART – B																																																		
1.	(i) Compare the diagram of a 4-bit SISO SIPO, PIPO and PISO shift register and draw its waveforms. (8) (ii) Realize D flip-flop using SR flip-flop. (5)	BTL5 BTL 2	Evaluating Understanding																																															
2.	(i) Construct a 4-bit down counter using logic gates. (5) (ii) Model a synchronous MOD-6 counter and explain with waveforms. (8)	BTL 3	Applying																																															
3.	How would you design the Sequential circuit has three flip flops A, B, and C; one input X_in ; and one output Y_out. The state diagram is shown in below figure. The circuit is to be designed by treating the unused states as don't care conditions. Analyze the circuit obtain from the design to determine the effect of the unused states. Use T flip flops in the design. (13)	BTL 1	Remembering																																															
4.	(i) Examine the number of state reduction in the following state table, and tabulate the reduced state table. (7)	BTL 4	Analyzing																																															
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Present state</th> <th colspan="2">Next State</th> <th colspan="2">Output</th> </tr> <tr> <th>X = 0</th> <th>X =1</th> <th>X =0</th> <th>X=1</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>F</td> <td>B</td> <td>0</td> <td>0</td> </tr> <tr> <td>B</td> <td>D</td> <td>C</td> <td>0</td> <td>0</td> </tr> <tr> <td>C</td> <td>F</td> <td>E</td> <td>0</td> <td>0</td> </tr> <tr> <td>D</td> <td>g</td> <td>A</td> <td>1</td> <td>0</td> </tr> <tr> <td>E</td> <td>d</td> <td>C</td> <td>0</td> <td>0</td> </tr> <tr> <td>F</td> <td>f</td> <td>B</td> <td>1</td> <td>1</td> </tr> <tr> <td>G</td> <td>g</td> <td>H</td> <td>0</td> <td>1</td> </tr> <tr> <td>H</td> <td>g</td> <td>H</td> <td>0</td> <td>1</td> </tr> </tbody> </table>			Present state	Next State		Output		X = 0	X =1	X =0	X=1	A	F	B	0	0	B	D	C	0	0	C	F	E	0	0	D	g	A	1	0	E	d	C	0	0	F	f	B	1	1	G	g	H	0	1	H	g	H
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5.	Analyze state reduction if possible after designing a clocked synchronous sequential logic circuit using JK flip flops for the following state diagram. Use state reduction if possible.(13)	BTL 4	Analyzing																																															
6.	(i) Show the operation of universal shift register with neat block diagram. (7) (ii) Estimate the design a counter to count the sequence 0, 1, 2, 4, 5, 6 ,.....using SR FF's. (6)	BTL 1 BTL 5	Remembering Evaluating																																															

7.	(i) Interpret design of a 3 bit synchronous counter using JK flip-flop. (10) (ii) Differentiate between a state table, characteristic table and an excitation table for D Flip Flop. (3)	BTL 3 BTL 2	Applying Understanding
8.	How would you describe the design of following: (i) Synchronous counter with states 0, 1, 2, 3, 0, 1,using JK flip flop. (7) (ii) Write short notes on Mealy and Moore sequential circuits . (6)	BTL 1	Remembering
9.	(i) Use T flip-flop to design counter with the following repeated binary sequence 0, 4, 7, 2, 3. (8) (ii) Realize JK Flip Flop using SR Flip Flop (5)	BTL 2 BTL 2	Understanding Understanding
10.	(i) Illustrate with diagram an asynchronous decade counter & its operation with neat waveforms. (7) (ii) Predict the design of a synchronous 3-bit counter which counts in the sequence 1, 3, 2, 6, 7, 5, 4, (repeat) 1, 3..... using T FF . (6)	BTL 1 BTL 2	Remembering Understanding
11.	Using SR flipflops design a parallel counter which counts in the sequence 000,111,101,110,001,010,000,... (13)	BTL 6	Creating
12.	(i) Discuss in detail about the pulse- triggered S-R Flip Flop with necessary diagrams. (7) (ii) Deduce a clocked synchronous sequential machine using T flip flops for the following state diagram. Use state reduction if possible .Also use straight binary state assignment. (6)	BTL 2 BTL 4	Understanding Analyzing
13.	(i) Using D flip-flop, Design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000. (10) (ii) Discuss the working of 4 bit Johnson counter with neat diagram. (3)	BTL 3 BTL 1	Applying Remembering
14.	(i) Point out a sequence detector design which detects the sequence 01110 using D flip flop. (7) (ii) Enumerate about Triggering of Flip-Flop. (6)	BTL 4 BTL 1	Analyzing Remembering
PART C			
1.	Design a J-K counter that goes through states 3,4, 6 , 7 and 3..... Is the counter self – starting ? Modify the circuit such that whenever it goes to an invalid state it comes back to state 3. (15)	BTL 6	Creating
2.	Explain the functions with the state diagram and characteristics equation of T FF, D FF and JK FF and compare and contrast among the FFs? (15)	BTL 5	Evaluating
3.	A sequential machine has one input line where 0's and 1's are being incident. The machine has to produce the output of '1' only when exactly two '0's are followed by '1' or exactly two '1's are followed by a '0'. Using any statement assignment in JK flipflop, synthesize the machine. (15)	BTL 6	Creating
4.	Determine the design of a clocked sequential machine using JK Flip Flops for the state diagram shown in figure. Use state reduction if possible and make proper state assignment. (15)	BTL 5	Evaluating

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS

Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Pulse mode sequential circuits, Design of Hazard free circuits.

PART A

Q. No	Questions	BT Level	Domain
1.	Mention the steps for the design of asynchronous sequential circuit?	BTL 1	Remembering
2.	Classify Asynchronous sequential circuits.	BTL 2	Understanding
3.	Bring out the difference between fundamental mode and pulse mode sequential circuits	BTL 4	Analyzing
4.	Define dynamic hazard? When do they occur?	BTL 3	Applying
5.	What are pulse mode circuits?	BTL 2	Understanding
6.	Distinguish between stable and unstable state.	BTL 4	Analyzing
7.	State the significance of state assignment?	BTL 2	Understanding
8.	Outline about asynchronous sequential circuit?	BTL 1	Remembering
9.	Illustrate about fundamental mode sequential circuit?	BTL 3	Applying
10.	Recall about Hazards? How it can be avoided?	BTL 1	Remembering
11.	Compare the ASM chart with a conventional flow chart.	BTL 2	Understanding
12.	Compile fundamental mode and pulse mode asynchronous sequential circuits.	BTL 6	Creating
13.	Analyze the causes of essential Hazard.	BTL 4	Analyzing
14.	Construct a combinational Hazard free circuits.	BTL 6	Creating
15.	Explain the analysis procedure of asynchronous sequential circuits.	BTL 5	Evaluating
16.	List the different techniques used in State assignment.	BTL 1	Remembering
17.	Model a Stable circuit and give one example.	BTL 3	Applying
18.	Identify the types of Hazards that exist in asynchronous sequential circuits.	BTL 1	Remembering
19.	Interpret critical race and give the methods for critical-race free state assignment.	BTL 5	Evaluating
20.	How can a race in digital circuits can be avoided?	BTL 1	Remembering

PART – B

1.	Design an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T=1 and C moves from 1 to 0. Otherwise the output is 0. (13)	BTL 6	Creating
2.	(i) What are the types of hazards? Check whether the following circuit contains a hazard or not $Y = X_1X_2 + X_2'X_3$. If the hazard is present, Demonstrate its removal. (13)	BTL 1	Remembering
3.	An asynchronous sequential circuit is described by the following excitation and output function. $Y = X_1X_2 + (X_1 + X_2) Y, Z = Y$. i. Draw the logic diagram. (3) ii. Derive the transition table and output map. (5) iii. Describe the behavior of the circuit (5)	BTL 4	Analyzing
4.	(i) What is a Hazard? Give hazard free realization for the following Boolean function. $F(A, B, C, D) = \sum m(1, 5, 6, 7)$ using AND-OR gate network. (10) (ii) Define Essential Hazards (3)	BTL 1	Remembering
5.	(i) Summarize the design procedure for a asynchronous sequential circuit. (10) (ii) Derive the state table of serial binary adder. (3)	BTL 2	Understanding
6.	Find a circuit that has no static hazards and implements the Boolean function $F(A, B, C, D) = \sum (0, 2, 6, 7, 8, 10, 12)$ using AND-OR logic. (13)	BTL 4	Analyzing
7.	Discuss the various problems arises in an asynchronous sequential circuits. Explain any two problems in detail. (13)	BTL 2	Understanding
8.	(i) Explain in detail about Races. (5) (ii) Explain the different methods of state assignment. (8)	BTL 4	Analyzing
9.	(i) Explain the fundamental mode asynchronous sequential circuit. (7) (ii) Explain the different types of Hazards. Design Hazard free circuits for $Y = X_1X_2 + X_2'Y$. (6)	BTL 5	Evaluating
10.	Define asynchronous sequential circuits, cycles, critical race and Non Critical race. (13)	BTL 1	Remembering

11.	Explain with neat diagram the different hazards and the way to eliminate them. (13)	BTL 3	Applying
12.	What is the objective of state assignment in a asynchronous circuits ?Give example circuit for hazard free realization. (13)	BTL 1	Remembering
13.	Classify the methods of Race Free State assignment and explain in detail. (13)	BTL 2	Understanding
14.	Design an Asynchronous sequential circuit with input A and B and an output Y. Initially at any time if both the inputs are 0, the output, Y=0 . When A or B = 1, Y =1. When the other input also become 1, Y=0. The output stays at 0 until circuit goes back to initial state. (13)	BTL 3	Applying

PART – C

1.	Design a asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is one, input X is transferred to Z. When Y is zero, the output does not change for any change in X. (15)	BTL 6	Creating
2.	Design a asynchronous D- type latch with two inputs C and D and output Q. Assume fundamental mode of operation. (15)	BTL 5	Evaluating
3.	Assess a circuit with primary inputs A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z = 1 it will remain so until A goes to 0. Draw timing diagram, state diagram, Primitive flow table for designing the circuit. (15)	BTL 6	Creating
4.	Construct an asynchronous circuit that will output only the first pulse received and will ignore other pulses. (15)	BTL 5	Evaluating

UNIT V MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS

Basic memory structure – ROM -PROM – EPROM – EEPROM –EAPROM, RAM – Static and dynamic RAM - Programmable Logic Devices – Programmable Logic Array (PLA) - Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) - Implementation of combinational logic circuits using PLA, PAL. Digital integrated circuits: Logic levels, propagation delay, power dissipation, fan-out and fan-in, noise margin, logic families and their characteristics-RTL, TTL, ECL, CMOS

PART A

Q.No	Questions	BT Level	Domain
1.	Compare and contrast the TTL, ECL gates.	BTL 2	Understanding
2.	Outline about CMOS logic circuits.	BTL 1	Remembering
3.	Point out the advantages of ECL.	BTL 4	Analyzing
4.	How does ROM retain information?	BTL 1	Remembering
5.	Distinguish between volatile and non-volatile memory.	BTL 2	Understanding
6.	Define propagation delay in logic gate.	BTL 1	Remembering
7.	Show the implementation of $Y = A + B'C$ using CMOS logic.	BTL 3	Applying
8.	Explain fan-in & fan-out of a standard TTL IC.	BTL 4	Analyzing
9.	Classify the different types of programmable logic device.	BTL 3	Applying
10.	State the advantages of FPGA.	BTL 1	Remembering
11.	Classify the logic gate families.	BTL 3	Applying
12.	What is programmable logic array? How it differs from ROM?	BTL 1	Remembering
13.	Implement the function $F1 = \sum (0, 1, 2, 5, 7)$ and $F2 = \sum (1, 2, 4, 6)$ using PROM.	BTL 4	Analyzing
14.	Enumerate about EPROM.	BTL 1	Remembering
15.	Generalize the implementation of 2 bit multiplier using ROM.	BTL 6	Creating
16.	Formulate the implementation of Ex OR function using PROM.	BTL 6	Creating
17.	Explain the advantages of EEPROM over EPROM.	BTL 5	Evaluating
18.	Describe various features of PROM, PAL and PLA.	BTL 2	Understanding
19.	Distinguish between PAL and PLA.	BTL 2	Understanding
20.	How the ECL logic is different from TTL?	BTL 5	Evaluating

PART – B

1.	(i) Describe about noise margin and propagation delay in logic gates (7) (ii) Construct a combinational circuit is defined as the function $F1 = AB'C'+AB'C+ABC$ and $F2 = A'BC+AB'C+ABC$. Implement the digital circuit with a PLA having 3 inputs, 3 Product terms and 2 outputs. (6)	BTL 1 BTL 4	Remembering Analyzing
2.	(i) Classify the types of PLDs and write notes on PLDs. (7) (ii) Implement the following Boolean function using $3 \times 4 \times 2$ PLA, $F1(x, y, z) = \sum (0, 1, 3, 5)$ and $F2(x, y, z) = \sum (3, 5, 7)$. (6)	BTL 2 BTL 3	Understanding Applying
3.	(i) Demonstrate the realization of the following function using PAL $F1(x, y, z) = \sum (1, 2, 4, 5, 7)$. And $F2(x, y, z) = \sum (0,1,3,5,7)$. (7) (ii) Write a notes on FPGA with neat diagram. (6)	BTL 2	Understanding
4.	(i) State the advantages of CMOS logic. (3) (ii) Analyze a combinational circuit using ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number. (10)	BTL 2 BTL 4	Understanding Analyzing
5.	Create the design of BCD to Excess 3 using PLA? (13)	BTL 6	Creating
6.	(i) Demonstrate the classification of semiconductor memories (7) (ii) Manipulate the function using PLA $F1 = \sum (2, 4, 5, 10, 12, 13, 14)$ and $F2 = \sum (2, 9, 10, 11, 13, 14, 15)$. (6)	BTL 3	Applying
7.	(i) Discuss the basic concepts and the principle of operation of Bipolar SRAM cell. (7) (ii) How can one make 64×8 ROM using 32×4 ROMs? Draw such a circuit & explain. (6)	BTL 3 BTL 4	Applying Analyzing
8.	How can you create the design of 32×8 ROM and give an explanation about it? (13)	BTL 4	Analyzing
9.	(i) Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working principle. (8) (ii) Realize the following function using PLA $F(w, x, y, z) = \Pi (0, 3, 5, 7, 12, 15) + d(2, 9)$. (5)	BTL 2	Understanding

10.	(i) Implement the switching functions. $z1 = \overline{abde} + \overline{abce} + bc + de$ $z2 = \overline{ace}$ $z3 = \overline{bc} + \overline{de} + \overline{cde} + bd \text{ and}$ $z4 = \overline{ace} + ce$ using a 5*8*4 PLA. (7) (ii) Write short notes on EPROM and EEPROM. (6)	BTL 5 BTL 1	Evaluating Remembering
11.	(i) Compare types of logic families and explain a short note on CMOS logic gate. (8) (ii) Implement the following function using PLA $F_1 = \sum (0, 1, 2, 4)$ and $F_2 = \sum (0, 5, 6, 7)$. (5)	BTL 4 BTL 5	Analyzing Evaluating
12.	Recognize the implementation of the following Boolean functions using $4 \times 3 \times 4$ PAL. (13) (i) $W(A,B,C,D) = \sum (0,2, 6,7,8,9,12,13)$ (ii) $X(A,B,C,D) = \sum (0, 2, 6, 7, 8, 9, 12, 13, 14)$ (iii) $Y(A, B, C, D) = \sum (2, 3, 8, 9, 10, 12, 13)$ (iv) $Z(A,B,C,D) = \sum (1, 3, 4, 6, 9, 12, 14)$	BTL 1	Remembering
13.	(i) Examine the structure of ECL and TTL (7) (ii) Outline about Tri state inverter configuration with neat diagram. (6)	BTL 1	Remembering
14.	(i) Explain EAPROM and static RAM cell using MOSFET? (5) (ii) Recognize 512 X 8 ROM using eight 64x8 ROM chips with an enable input and a decoder? (8)	BTL 1	Remembering
PART C			
1.	Design a combinational circuit using CMOS logic. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number. (15)	BTL 6	Creating
2.	Develop the code converters using PROM devices. (15) (i) Binary to gray code (ii) Gray to Binary code	BTL 5	Evaluating
3.	(i) Interpret how does Programmable logic devices differ from FPGA? (8) (ii) Formulate the implementation of the following functions with PLA having three inputs, four product terms, and two outputs. $F_1 (A, B, C) = (3, 5, 6, 7)$ $F_2 (A, B, C) = (0, 2, 4, 7)$ (7)	BTL 5	Evaluating
4.	Build the structure of PAL and PLA. How a combinational logic function is implemented in PAL and PLA? Explain with an example for each. (15)	BTL 6	Creating